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UNIVERSITY COLLEGE, CORK

Spring 2006
Third Engineering (Microelectronics) Examination

Analogue Integrated Circuits (UE3003)

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Attempt five questions, at least two from each Section (3 HOURS)
(Approved calculator allowed)

Questions follow overleaf

Section A

Question 1 [20 marks]

Calculate the fan-out of the DTL gate shown in Fig. 1, assuming $V_{CC} = 5$ V, $R_1 = 2.2$ kΩ, $R_2 = 1.2$ kΩ, $R_3 = 2.2$ kΩ, $R_4 = 1.2$ kΩ, $V_{D(ON)} = V_{BE(sat)} = 0.7$ V, $V_{CE(sat)} = 0.2$ V, $\beta_F = 20$, and $\beta_R = 0.2$.

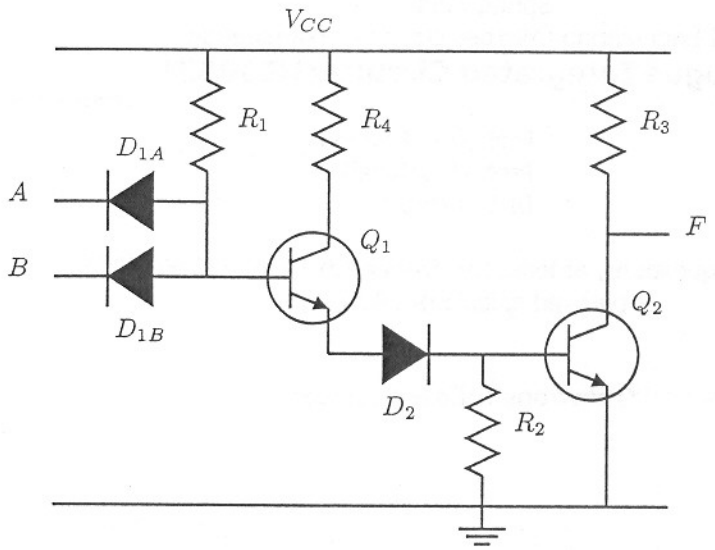

Figure 1

Your solution is correct!

N = 37

call current

LOAD NOT Id(gate)

~ 125 µ

Question 2 [20 marks]

You have been asked to design a NOT gate in a 0.8 µm CMOS process The process parameters are: $V_{tn} = 0.7$ V, $V_{tp} = -0.9$ V; $\mu_n = 500$ cm^2/Vs, $\mu_p = 175$ cm^2/Vs; $t_{ox} = 18$ nm. The power supplies are: $V_{DD} = 5$ V, $V_{SS} = 0$ V.

correct!

(a) Sketch the circuit diagram of your inverter, showing all four terminals for each transistor.

(b) Using driving-point characteristics and load "lines" (or otherwise), explain the operation of the circuit. correct diag. 24/11/05 & SEDRA

(c) Sketch the input-output voltage transfer characteristic, indicating the regions of operation of each transistor. ALSO CORRECT & in SEDRA

d (d) Derive an expression for the switching threshold V_{th}. CORRECT

typo e (e) Using the result of (c), select the widths of minimum-length transistors such that $V_{th} = V_{DD}/2$. $L_p = L_n = W_n$, only W_p needs be scaled up!

f (f) Sketch the circuit diagram of a NAND gate in the same CMOS process, indicating the sizes of the transistors that give $V_{th} = V_{DD}/2$. Show all four connections per transistor.

→ twice as long

needs 2W for n-type MOS

"2" L

*

Question 3 [20 marks]

Figure 3 shows a differential amplifier. $V_{CC} = V_{EE} = 5$ V, $R_{C_1} = R_{C_2} = 5.6$ kΩ, $R_{REF} = 6.8$ kΩ, $R_3 = R_4 = 2.4$ kΩ. You may assume that all transistors are identical, with $V_{BE(ON)} = 0.7$ V, $V_A = 100$ V, and $\beta_F = 250$. Define $V_i = V_{i_1} - V_{i_2}$ and $V_o = V_{o_1} - V_{o_2}$. Calculate:

(a) The operating point; V_{CE}

(b) The small-signal differential voltage gain v_{o_d}/v_{i_d};

(c) The small-signal common-mode voltage gain v_{o_c}/v_{i_c};

(d) The CMRR, expressed in dB. $\frac{a_d}{a_c}$

} can simply write down formulae for this

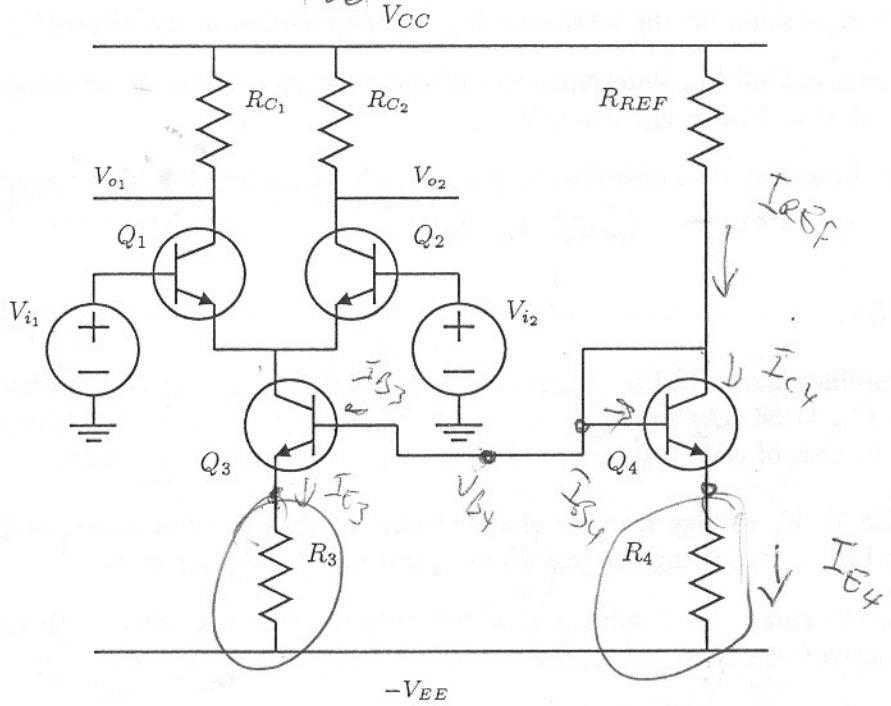

Figure 3

(a) See explanatory sheet for voltage calc.

(b) S.S. voltage gain eqn! ✓

(c) eqn ✓

(d) CMRR calc.

Design Exp.

Section B

Question 4 [20 marks]

You have been asked to design an analogue switch in a 0.25 μm CMOS process The process parameters are: V_{tn} = 0.43 V, V_{tp} = -0.62 V; $\mu_n C_{ox}$ = 267 μA/V^2, $\mu_p C_{ox}$ = 93 μA/V^2. The power supplies are: V_{DD} = 2.5 V, $-V_{SS}$ = -2.5 V.

(a) Sketch the circuit diagram of your analogue switch, showing all four terminals for all transistors. Indicate clearly the logic control lines. Show just switch & control lines

(b) Explain the operation of your circuit.

(c) Derive an expression for the resistance R_{ON} of your switch in the "closed" position. Look up!

(d) Using the result of (c), determine the W/L ratios of the switch transistors such that $R_{ON} < 50\ \Omega$ at $V_{IN} \approx V_{OUT} = 0$ V.

(e) Estimate the silicon area occupied by your switch (excluding the logic circuitry).
— Area in notes — based on calc.

triode region

large I for sm. V

"ohmic"

Question 5 [20 marks]

The CMOS amplifier shown in Fig. 5 has W/L = 7.2 μm/0.36 μm for all transistors, $\mu_n C_{ox}$ = 387 μA/V^2, $\mu_p C_{ox}$ = 86 μA/V^2, I_{REF} = 50 μA, V_{An} = 5 V, $|V_{Ap}|$ = 6 V. Furthermore, the parasitic capacitances of each transistor are given by C_{gs} = 20 fF, C_{gd} = 5 fF.

Correct!

(a) Sketch the V_i–V_o voltage transfer characteristic of the common-source amplifier circuit shown in Fig. 5, indicating the regions of operation of the transistors.

(b) Calculate the small-signal voltage gain and output resistance when both transistors are forward active. $r_o = (r_{o3} \parallel R_L) \longrightarrow R_L = r_{o2}$ $A_V = \frac{v_o}{v_i}$

(c) Assuming that the amplifier is driven by a real voltage source V_s with series resistance R_s = 10 kΩ, and a load capacitance C_L = 25 fF is connected across V_o, sketch the frequency response V_o/V_s, and calculate the -3 dB frequency f_H.

Look up

$\omega_{ta} = \frac{-g_m}{C_c}$

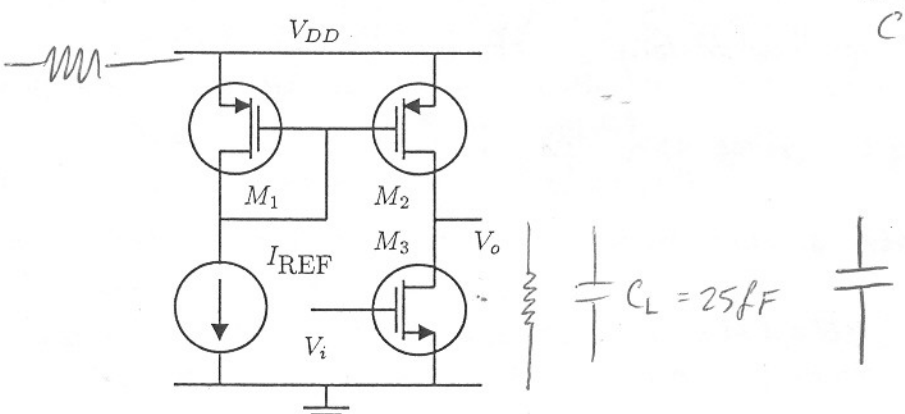

Figure 5

$f_H = \frac{1}{2\pi C_L r_o}$

-20dB/dec

-40dB/dec

Question 6 [20 marks]

Consider the circuit in Fig. 6. with the following device geometries.

Transistor	M1	M2	M3	M4	M5	M6	M7	M8
W/L	120/8	120/8	50/10	50/10	150/10	100/10	W_7/10	300/10

Let $I_{REF} = 50\ \mu A$, $C_C = 10$ pF, $|V_t| = 1$ V for all devices, $\mu_n C_{ox} = 20\ \mu A/V^2$, $\mu_p C_{ox} = 10\ \mu A/V^2$, $|V_A| = 25$ V for all devices, $V_{DD} = 5$ V, $V_{SS} = 5$ V.

(a) Choose the value of W_7 such that this circuit does *not* exhibit a systematic offset voltage.

(b) Using the value of W_7 in (a), evaluate I_D, $|V_{GS}|$, g_m and r_o for all devices. Hint: You may neglect the effect of V_A when calculating the bias currents.

(c) Calculate the DC open-loop voltage gain of the amplifier.

(d) Calculate the slew rate of the amplifier.

(e) Calculate the -3 dB frequency of the amplifier.

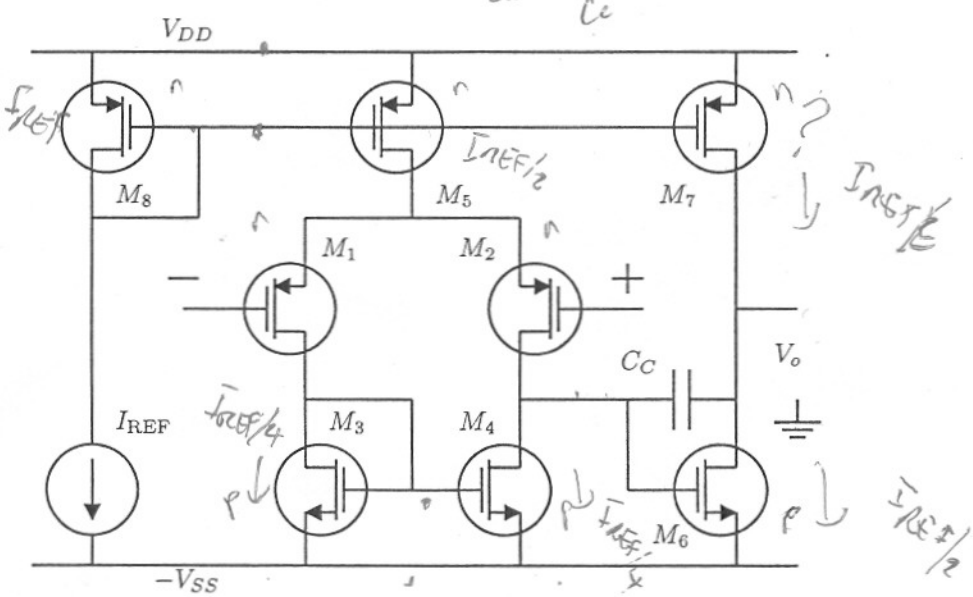

Figure 6

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