NEW PART

Section A

Question 1 [20 marks]

Figure 1 shows a DTL gate.

(a) Calculate the fan-out of this gate assuming $V_{CC} = 4$ V, $V_{D(ON)} = V_{BE(sat)} = 0.7$ V, $V_{CE(sat)} = 0.2$ V, and $\beta_F = 25$.

NEW (b) What is the principal disadvantage of this circuit and how could it be rectified?

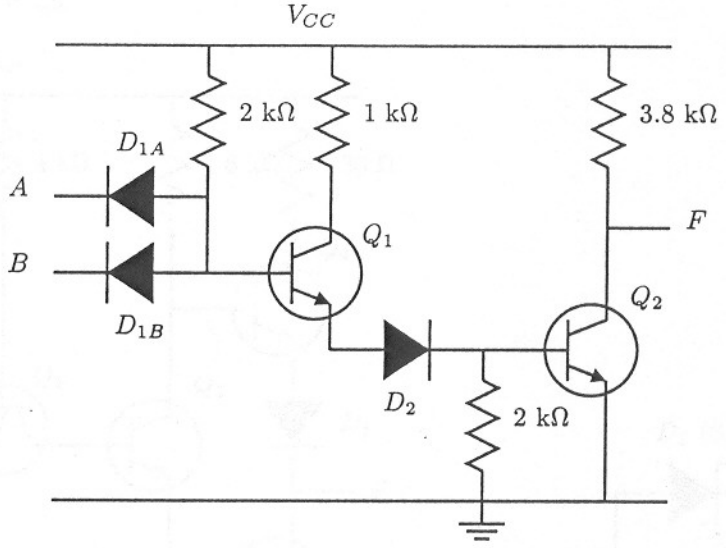
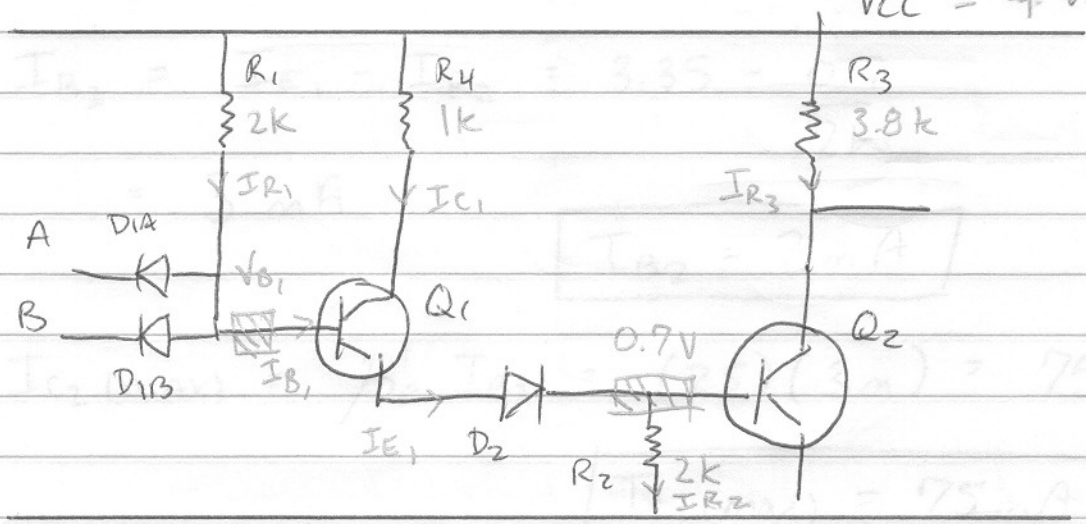


Figure 1

Aut 2005 Q1 10/8/06

DTL gate fan-out $\beta_F = 25$

SEE BACK IMPORTANT ALT. @



$V_{B_1} = V_{BE(sat)_2} + V_{D_{on}} + V_{BE(sat)_1}$

$= 2.1\ V$

$\boxed{V_{B_1} = 2.1\ V}$

$I_{B_1} = \frac{V_{cc} - V_{B_1}}{R_1} = \frac{4 - 2.1}{2k} = 0.95\ mA$

$\boxed{I_{B_1} = 0.95\ mA}$

Assuming Q_1 not saturated

$I_{C_1} = \beta_F I_{B_1} = (25)(0.95m) = 23.75\ mA$

$\boxed{I_{C_1} = 23.75\ mA}$

$V_{C_1} = V_{cc} - R_4 I_{C_1}$

$= 4 - (1k)(23.75m)$

$= -19.75\ V$ So Q_1 IS Sat.

hence $V_{C_1} = V_{BE(sat)_2} + V_D + V_{CE(sat)_1} = 1.6\ V$

$\boxed{V_{C_1} = 1.6\ V}$

$I_{C_1} = \frac{V_{cc} - V_{C_1}}{R_4} = \frac{4 - 1.6}{1} = 2.4\ mA$

$\boxed{I_{C_1} = 2.4\ mA}$

$I_{E_1} = I_{B_1} + I_{C_1} = 0.95\,mA + 2.40\,mA$

$= 3.35\,mA$

$\boxed{I_{E_1} = 3.35\,mA}$

$I_{B_2} = I_{E_1} - I_{R_2} = 3.35 - \frac{0.7}{2k}$

$= 3\,mA$

$\boxed{I_{B_2} = 3\,mA}$

$I_{C_2(MAX)} = \beta_F I_{B_2} = (25)(3m) = 75\,mA$

$\boxed{I_{C_2(max)} = 75\,mA}$

$I_{R_3} = \frac{V_{CC} - V_{CE(sat)_2}}{R_3} = \frac{4 - 0.2}{3.8k} = 1\,mA$

$\boxed{I_{R_3} = 1\,mA}$

$I_{LOAD} = \frac{V_{CC} - V_D - V_{CE_2}}{R_1} = \frac{4 - 0.9}{2k} = 1.55\,mA$

$\boxed{I_{LOAD} = 1.55\,mA}$

$I_{C_2(MAX)} = N I_{LOAD} + I_{R_3}$

$75m = N(1.55m) + 1$

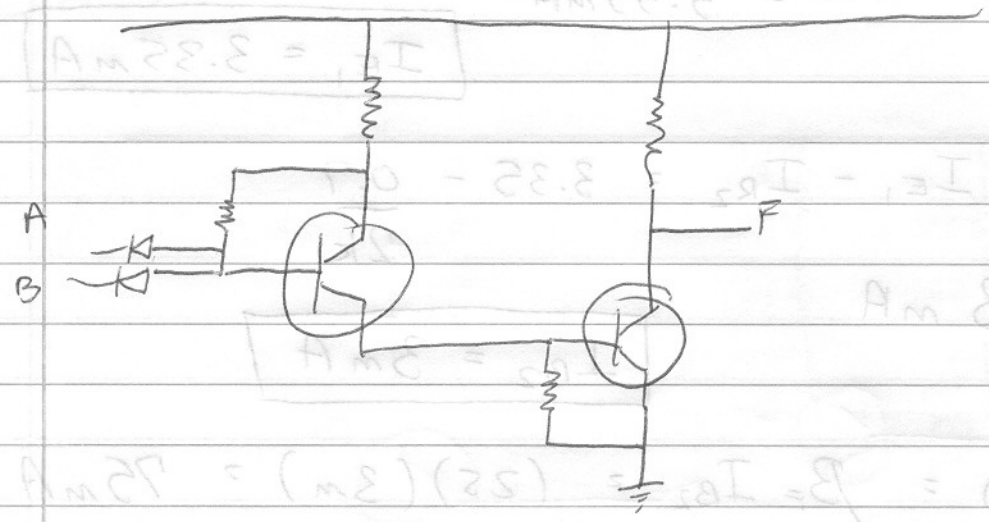
$N = 47.74$, FANOUT $\boxed{N = 47}$

Q completed in 11:26

(b) ① Long propagation delay time when Q_2 turns off

Principal disadvantage ~~is the long propagation delay and~~

② poor switching speed ~~when Q_2 is off.~~ → Rectify w/ mod. DTL gate



form of feedback biasing to prevent Q_1 from saturating