

NEW PART

Section A

Question 1

[20 marks]

Figure 1 shows a DTL gate.

(a) Calculate the fan-out of this gate assuming $V_{CC} = 4\text{ V}$, $V_{D(ON)} = V_{BE(sat)} = 0.7\text{ V}$, $V_{CE(sat)} = 0.2\text{ V}$, and $\beta_F = 25$.

NEW (b) What is the principal disadvantage of this circuit and how could it be rectified?

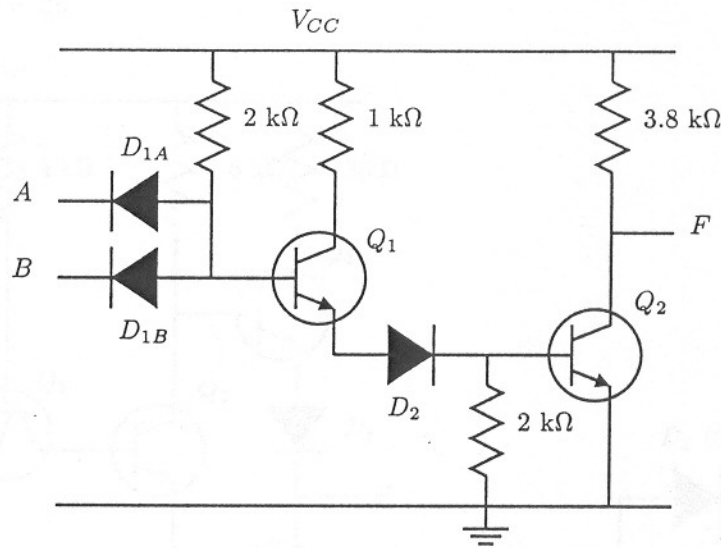


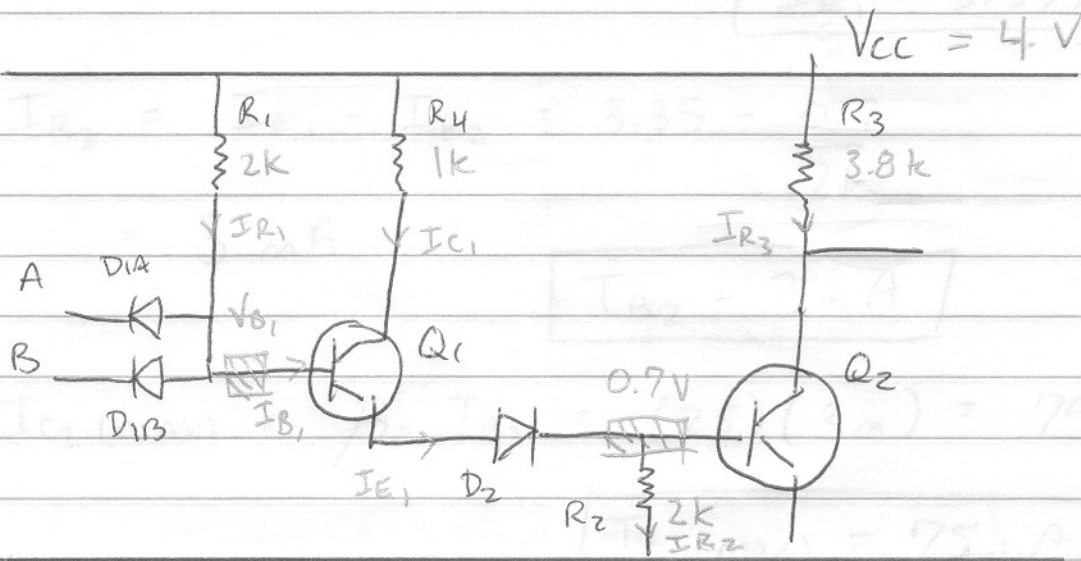
Figure 1

Aut 2005 Q1

10/8/06

DTL gate fan-out = 3.35 $\beta_F = 25$

SEE BACK IMPORTANT ALT.



$$V_{B1} = V_{BE(sat)2} + V_D + V_{BE(sat)1}$$

$$= 2.1 \text{ V}$$

$$V_{B1} = 2.1 \text{ V}$$

$$I_{B1} = \frac{V_{CC} - V_{B1}}{R_1} = \frac{4 - 2.1}{2k} = 0.95 \text{ mA}$$

$$I_{B1} = 0.95 \text{ mA}$$

Assuming Q_1 not saturated

$$I_{C1} = \beta_F I_{B1} = (25)(0.95 \text{ mA}) = 23.75 \text{ mA}$$

$$I_{C1} = 23.75 \text{ mA}$$

$$V_{C1} = V_{CC} - R_4 I_{C1}$$

$$= 4 - (1k)(23.75 \text{ mA})$$

$$= -19.75 \text{ V}$$

So Q_1 is sat.

hence $V_{C1} = V_{BE(sat)2} + V_D + V_{BE(sat)1} = 1.6 \text{ V}$

$$V_{C1} = 1.6 \text{ V}$$

$$I_{C1} = \frac{V_{CC} - V_{C1}}{R_4} = \frac{4 - 1.6}{1} = 2.4 \text{ mA}$$

$$I_{C1} = 2.4 \text{ mA}$$

$$I_{E1} = I_{B1} + I_{C1} = 0.95 \text{ mA} + 2.40 \text{ mA} \\ = 3.35 \text{ mA}$$

$$I_{E1} = 3.35 \text{ mA}$$

$$I_{B2} = I_{E1} - I_{R2} = 3.35 - \frac{0.7}{2k} \\ = 3 \text{ mA}$$

$$I_{B2} = 3 \text{ mA}$$

$$I_{C2}(\text{MAX}) = \beta_F I_{B2} = (25)(3 \text{ mA}) = 75 \text{ mA}$$

$$I_{C2}(\text{MAX}) = 75 \text{ mA}$$

$$I_{R3} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_3} = \frac{4 - 0.2}{3.8k} = 1 \text{ mA}$$

$$I_{R3} = 1 \text{ mA}$$

$$I_{\text{LOAD}} = \frac{V_{CC} - V_D - V_{CE2}}{R_1} = \frac{4 - 0.9}{2k} = 1.55 \text{ mA}$$

$$I_{\text{LOAD}} = 1.55 \text{ mA}$$

$$I_{C2}(\text{MAX}) = N I_{\text{LOAD}} + I_{R3}$$

$$75 \text{ mA} = N(1.55 \text{ mA}) + 1$$

$$N = 47.74$$

$$N = 47$$

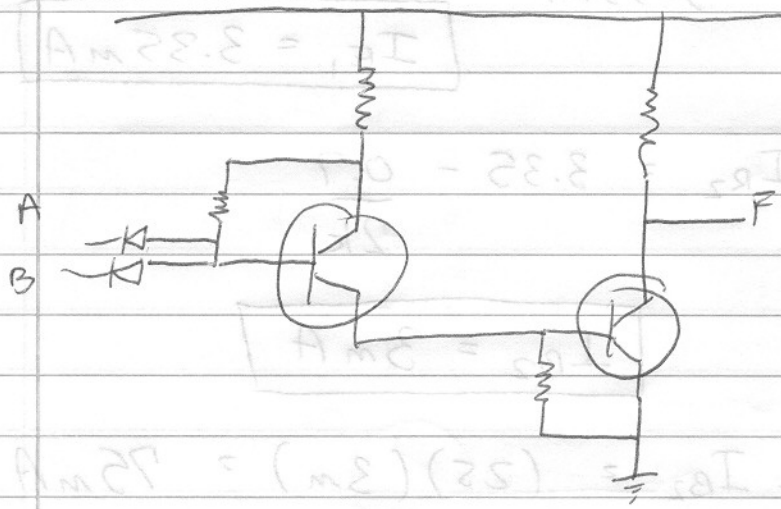
$I_{C1} Q$ completed in 11:26 = 2.4 mA

① Long propagation delay time when Q_2 turns off

(b) Principal disadvantage is the long propagation delay and

② poor switching speed when Q_2 is off. \rightarrow Rectify w/ mod. DTL gate

$$I_{E1} = I_{B1} + I_{C1} = 0.02 \text{ mA} + 2.40 \text{ mA} = 2.42 \text{ mA}$$



form of feedback biasing to prevent Q_1 from saturating

$$I_{R2} = \frac{V_{CC} - V_{BE} - V_D}{R_2} = \frac{5.0 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V}}{3.8 \text{ k}\Omega} = 0.8 \text{ mA}$$

$$I_{R2} = 1 \text{ mA}$$

$$I_{\text{load}} = \frac{V_{CC} - V_D - V_{CEs}}{R_1} = \frac{5.0 \text{ V} - 0.7 \text{ V} - 1.2 \text{ V}}{2 \text{ k}\Omega} = 1.55 \text{ mA}$$

$$I_{\text{load}} = 1.22 \text{ mA}$$

$$I_{C2(\text{max})} = I_{R2} + I_{\text{load}} = 0.8 \text{ mA} + 1.22 \text{ mA} = 2.02 \text{ mA}$$

$$I_{C2} = I_{C2(\text{max})} = 2.02 \text{ mA}$$

$$N = 47$$

$$N = 47.74$$

- ① Long propagation delay from when Q_2 turns off
- ② Poor switch speed when Q_2 is off
- ③ Principal disadvantage is the long propagation delay and
- ④ completed in 11:50